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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,167	06/14/2001	Richard A. Skogman	15436.435.5	6849

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EXAMINER	
AL NAZER, LEITH A	
ART UNIT	**PAPER NUMBER**
2821	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,167	SKOGMAN, RICHARD A.	
	Examiner	Art Unit	
	Leith A Al-Nazer	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 10-15, 17-19, and 24-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson '683.

With respect to claims 1, 14, and 15, Johnson teaches a substrate (14); a laser area comprising a bottom semiconductor DBR stack (58), an active region (64 and 66), and a partial top semiconductor DBR stack (68; column 7, lines 28-50) positioned upon the substrate; a dielectric mirror (90) forming an aperture area and being positioned upon the partial top semiconductor DBR stack; and an implanted region (76 and 82) configured around the aperture area but not penetrating the aperture area.

With respect to claim 2, Johnson shows epitaxially grown layers comprising a bottom semiconductor DBR stack, an active region, and a top semiconductor DBR stack (figures 3-5).

With respect to claims 3 and 17, Johnson teaches the top semiconductor DBR stack containing material chosen from the group consisting of aluminum, gallium, arsenic, indium, phosphorous, and combinations thereof (column 2, lines 28-31).

With respect to claims 4 and 18, Johnson teaches the top semiconductor DBR stack comprising alternating layers of aluminum gallium arsenide and aluminum arsenide (column 2, lines 28-31).

With respect to claims 5 and 19, Johnson teaches the top semiconductor DBR stack being doped (column 2, lines 31-34).

With respect to claims 10-12 and 24-26, Johnson teaches the dielectric material being chosen from the group consisting of silicon dioxide, titanium dioxide, silicon nitride, and combinations thereof (figures 3-5).

With respect to claims 13 and 27, Johnson teaches the device being a vertical cavity surface-emitting laser (figures 1 and 3-5).

With respect to claims 28 and 30, Johnson teaches a vertical cavity surface emitting laser comprising a substrate (14); a bottom semiconductor DBR stack (58); an active region (64 and 66) comprising an aperture where light is emitted; a top semiconductor DBR stack (68); and a dielectric mirror (90) positioned directly on the top semiconductor DBR stack over the aperture of the active region, wherein the bottom semiconductor DBR stack and the top semiconductor DBR stack comprise epitaxial layers and the bottom semiconductor DBR stack comprises more epitaxial layers than the top semiconductor DBR stack (column 7, lines 28-50).

With respect to claim 29, Johnson teaches the number of epitaxial layers comprising the top semiconductor DBR stack being less than 5% of the number of epitaxial layers comprising the bottom semiconductor DBR stack (column 7, lines 28-50).

Claim 31 requires the bottom DBR stack and the top DBR stack have certain reflectivities and the reflectivity of the bottom DBR stack is higher than the reflectivity of the top DBR stack. Although not explicitly stated, such a setup is inherent in the device of Johnson. The light is emitted from the top semiconductor DBR stack. Therefore, it must have a lower reflectivity than the bottom DBR stack.

With respect to claim 32, Johnson teaches a VCSEL comprising a substrate (14); a bottom semiconductor DBR stack (58); an active region (64 and 66) comprising an aperture area where light is emitted; a top semiconductor DBR stack (68); an implanted region (82) within the epitaxial layers, the implanted region configured around the aperture area but not penetrating the aperture area (figures 3-5); and a dielectric mirror (90) positioned directly on the top semiconductor DBR stack over the aperture area of the active region, the dielectric mirror functioning as a guide to form the implanted region (column 7, lines 28-50); wherein the bottom semiconductor DBR stack and the top semiconductor DBR stack comprise epitaxial layers and the bottom semiconductor DBR stack comprises more epitaxial layers than the top semiconductor DBR stack (column 7, lines 28-50).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5 Claims 6-9, 20-23, and 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson '683 in view of Sun '241.

Claims 6, 20, and 39 require the top semiconductor DBR have forty individual layers or less. Sun teaches such a setup (column 2, lines 30-35). At the time of the invention, it would have been obvious to one having ordinary skill in the art to take the system of Johnson and specify forty or less individual layers. The motivation for doing so would have been to provide a DBR mirror stack with a desired reflectivity.

Claims 7, 21, and 40 require the top semiconductor DBR have twenty individual layers or less. Sun teaches such a setup (column 2, lines 30-35). At the time of the invention, it would have been obvious to one having ordinary skill in the art to take the system of Johnson and specify forty or less individual layers. The motivation for doing so would have been to provide a DBR mirror stack with a desired reflectivity.

Claims 8, 22, and 41 require the top semiconductor DBR have eleven individual layers or less. Sun teaches such a setup (column 2, lines 30-35). At the time of the invention, it would have been obvious to one having ordinary skill in the art to take the

system of Johnson and specify forty or less individual layers. The motivation for doing so would have been to provide a DBR mirror stack with a desired reflectivity.

Claims 9, 23, and 42 requires the top semiconductor DBR have seven individual layers or less. Sun teaches a similar top DBR with ten layers (column 2, lines 30-35). It is well known in the art that one can vary the number of top DBR layers in order to obtain a top DBR with a desired reflectivity. Therefore, it would have been obvious to one having ordinary skill in the art to provide the system of Johnson or Sun with a DBR of seven or less layers. The motivation for doing so would have been to provide a top DBR with a desired reflectivity.

6. Claims 33-38 and 43-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson '683 in view of Lott et al.

With respect to claims 33-35, Johnson teaches a laser comprising a substrate (14); a bottom semiconductor DBR stack (58); an active region (64 and 66) positioned upon the bottom semiconductor DBR stack; a partial top semiconductor DBR stack (68) positioned upon the active region; a dielectric mirror (90) forming an aperture area and being positioned upon the partial top semiconductor DBR stack; and an implanted region (76 and 82) configured around the aperture area but not penetrating the aperture area. Claim 33 requires the aperture area have a width of about 2 to 25 micrometers. Such dimensions are common in the art, as is evidenced by Lott (page 1397, column 2). At the time of the invention, it would have been obvious to one having ordinary skill in the art to take the system of Johnson and specify an aperture of about 2 to 25

micrometers as taught by Lott. The motivation for doing so would have been to provide an aperture with optimal dimensions for device operation and fabrication, such as ion implantation.

With respect to claim 36, Johnson teaches the top semiconductor DBR stack containing material chosen from the group consisting of aluminum, gallium, arsenic, indium, phosphorous, and combinations thereof (column 2, lines 28-31).

With respect to claim 37, Johnson teaches the top semiconductor DBR stack comprising alternating layers of aluminum gallium arsenide and aluminum arsenide (column 2, lines 28-31).

With respect to claim 38, Johnson teaches the top semiconductor DBR stack being doped (column 2, lines 31-34).

With respect to claims 43-45, Johnson teaches the dielectric material being chosen from the group consisting of silicon dioxide, titanium dioxide, silicon nitride, and combinations thereof (figures 3-5).

With respect to claim 46, Johnson teaches the device being a vertical cavity surface-emitting laser (figures 1 and 3-5).

Response to Arguments

7. Applicant's arguments filed 18 June 2004 have been fully considered but they are not persuasive.

Examiner has withdrawn the 35 USC 102 rejection over Lott and the 35 USC 102 rejection over Sun. However, the 35 USC 102 rejection over Johnson still stands.

Applicant argues that Johnson does not teach a dielectric mirror forming an aperture area and being positioned upon the partial top semiconductor DBR stack; and an implanted region configured around the aperture area but not penetrating the aperture area. Examiner disagrees. Figures 3-5 of Johnson clearly show a dielectric mirror (90) forming an aperture area and being positioned upon a partial top semiconductor DBR stack (68); and an implanted region (82) configured around the aperture area but not penetrating the aperture area.

Communication Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leith A Al-Nazer whose telephone number is 571-272-1938. The examiner can normally be reached on Monday-Friday, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LA

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